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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,074	11/03/2003	Evan Downey	127072	3723

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,074	DOWNEY ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-22 and 24-28* is/are allowed.

6)☒ Claim(s) *1-5 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 11 is objected to because of the following informalities:

lines 2-3, replace "correlative two power connections" with – correlative to power connections --;

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 and 23 are rejected under 35 U.S.C. 102(e) as being unpatentable by Khazei et al. (US Patent 6,834,380).

3. As to claims 1 and 23 Khazei discloses:

(1) A method of modeling a light emitting diode device (semiconductor chip) comprising:

automatically generating a netlist from a computer-aided design layout (FIG. 70 shows a flowchart for an automated component placement tool, which translates a logical or schematic circuit description into a template/netlist for the placement of components within an actual prototype... The tool may also receive data such as

constraints on the size and/or shape of the finished prototype. When used to design integrated circuits, automated placement tools are also called floorplanners – col.1, ll.26-48) (col.1, ll.26-48; col.33, ll.48-64); and

executing the netlist (In task P130 an electromagnetic field is calculated. In addition to the data received in task P120, this field calculation is performed with reference to one or more emissions profiles that correspond to the circuit components. These emissions profiles are mathematically modeled, and may be provided as a library or database- col.33, ll.65-67; col.34, ll.1-5) to produce an output correlative to current spreading uniformity for the light emitting diode device (collected data may be displayed as, e.g., power distributed over a preselected area; contour plots of current density distribution over the surface of the semiconductor chip device- col.19, ll.54-59 (col.19, ll.54-67; col.20, ll.1-14; col.20, ll.36-44; col.33, ll.65-67; col.34, ll.1-36; col.35, ll.18-30);

(23) A computer-readable medium storing computer instructions (col.41, ll.16-32) for:

automatically generating a netlist from a computer-aided design layout corresponding to a light emitting diode device (FIG. 70 shows a flowchart for an automated component placement tool, which translates a logical or schematic circuit description into a template/netlist for the placement of components within an actual prototype... The tool may also receive data such as constraints on the size and/or shape of the finished prototype. When used to design integrated circuits, automated placement tools are also called floorplanners – col.1, ll.26-48) (col.1, ll.26-48; col.33, ll.48-64).

4. As to claims 3-5 Khazei recites:

(3) The method comprising producing a plurality of contour plots correlative to the current spreading uniformity for the light emitting diode device (col.19, ll.54-67; col.20, ll.1-14);

(4) the method comprising producing an output correlative to thermal performance of the light emitting diode device (col.20, ll.36-44);

(5) the method comprising producing an output correlative to optical performance of the light emitting diode device (col.41, ll.16-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khazei in view of Igusa et al. (US Patent 6,865,726).

With respect to claim 2 Khazei teaches the features above but lacks a method of modeling a light emitting diode device (semiconductor chip), wherein automatically generated a netlist comprises at least 60,000 lines.

As to claim 2 Igusa in view of Khazei teaches:

the method comprises automatically generating a netlist having at least 60,000 lines (col.11, ll.28-67; col.12, ll.1-17).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Igusa's teaching regarding the method of modeling a light emitting diode device (semiconductor chip), wherein automatically generated a netlist comprises at least 60,000 lines and use it in Khazei's invention to process larger size netlists, thereby increasing an efficiency of the modeling large semiconductor chips, e.g., light emitting diodes.

Allowable Subject Matter

6. Claims 10-15 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A method of modeling a light emitting diode device comprising: scaling the layout to a specified element size, wherein the scaled layout includes each of a plurality of nodes, a plurality of resistors and a plurality of diodes each having a layer number and a unique coordinate associated therewith; automatically generating a netlist from the scaled layout; and executing the netlist to produce an output correlative to current spreading uniformity for the light emitting diode device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STACY A. WHITMORE
PRIMARY EXAMINER

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